CLAIMS:

1. A method of synchronizing a phase lock loop to an intermittent clock signal, the method comprising the steps of:

(A) seeking to acquire phase lock during periods of the intermittent clock; and

(B) holding the phase lock loop in a free-running state during periods when the intermittent clock is absent.

2. The method according to claim 1, further comprising the steps of:

(C) acquiring frequency lock in an asynchronous mode.

3. The method according to claim 1, wherein the intermittent clock signal is derived from a geometric eccentricity associated with a track on an optical disc and the geometric eccentricity is interspersed by regularly spaced header regions that disrupt the geometric eccentricity.

4. The method according to claim 3, further comprising:

timing a duration of the intermittent clock signal; and

placing the phase lock loop in the free-running state in anticipation of an arrival of a header in response to an elapsed duration of the intermittent clock signal.

5. The method according to claim 4, further comprising:

identifying re-emergence of the intermittent clock signal; and

seeking to acquire phase lock only after re-emergence of the intermittent clock signal has been validated.

6. The method according to claim 3, further comprising:

estimating a signal envelope for the intermittent clock signal;

bandpass filtering the header region to generate a spike indicative of a header transition;

amplifying the signal envelope and the spike to scale the spike relative to the signal envelope to differentiate the signal envelope from the spike;

defining a threshold exceeding the signal envelope; and

identifying commencement of a header region by equating a first spike transition through the threshold as being indicative of the header region.

7. The method according to claim 6, further comprising:

identifying a relative signal level polarity between a first spike and a successive spike to identify a requirement for a phase reversal.

8. The method according to claim 6, further comprising:

filtering the intermittent clock signal in a low pass filter to generate an adaptive slice level signal capable of tracking residual near-DC variations in the intermittent clock signal.

9. A computer readable medium configured to execute the steps of claim 1.

10. A control circuit coupled to a phase lock loop arranged to receive an intermittent clock signal to which the phase lock loop is to be synchronized, the control circuit configured to maintain operation control of the phase lock loop, determine periods of time when the intermittent clocking signal is stable, selectively maintain the phase lock loop in a phase acquisition state during said periods of time, and force the phase lock loop to enter a free-running state during periods of time when the intermittent clock signal is absent or not stable.

11. The control circuit of claim10, wherein the intermittent clock signal is derived from a geometric eccentricity associated with a track on an optical disc and the geometric eccentricity is interspersed by regularly spaced header regions that disrupt the geometric eccentricity and which each define a data sector, the control circuit further comprising:

a counter arranged to time the intermittent clock signal during each data sector, wherein the control circuit is further configured to force the phase lock loop to enter a free-running state being operationally in response to time elapsed within each data sector and the phase lock loop is placed in the free-running state, based on time elapsed, in advance of an arrival of a header.

12. The control circuit of claim 11, further comprising:

a detector arranged to identify emergence of a steady state in the intermittent clock signal, wherein the control circuit is further configured to force the phase lock loop to enter the free-running state, being operationally disabled by the detector, in response to the steady state.

13. The control circuit of claim 11, further comprising:

a top hold feedback circuit arranged to estimate a signal envelope for the intermittent clock signal;

a bandpass filter configured to receive the intermittent clock signal, the bandpass filter arranged to filter the header region to generate a spike indicative of a header transition;

an amplifier configuration arranged to amplify the signal envelope and the spike, to scale the spike relative to the signal envelope to differentiate the signal envelope from the spike;

a data slicing circuit configured to define a threshold exceeding the signal envelope; and

a comparator arrangement arranged to identify commencement of a header region by equating a first spike transition through the threshold as being indicative of the header region.

14. The control circuit of claim 13, wherein the comparator arrangement comprises first and second comparators configured to process opposite signal senses from the signal envelope, the first and second comparators each providing an output to a controller arranged to identify the relative signal level polarity between a first spike and a successive spike to identify a requirement for a phase reversal in the phase lock loop.

15. The control circuit of claim 12, further comprising:

a low pass filter arranged to generate an adaptive slice level signal capable of tracking residual DC variations in the intermittent clock signal in response to a filtered clock signal.

16. A DVD-RAM read channel comprising:

an array of photodiodes adapted to recover a push-pull signal representation from an optical disc containing data segments interspersed with header regions; and

a bandpass filter configured to receive the push-pull signal representation and filter the header region to generate a spike indicative of a header transition.

17. The DVD-RAM read channel of claim 16, further comprising:

a low pass filter, configured to generate an adaptive slice level signal capable of tracking residual DC variations in the push-pull signal in response to a wobble signal emanating from the bandpass filter.

18. The DVD-RAM read channel of claim 16, further comprising:

a top hold feedback circuit arranged to estimate a signal envelope for an intermittent clock signal;

an amplifier configuration arranged to amplify the signal envelope and the spike to scale the spike relative to the signal envelope to differentiate the signal envelope from the spike;

a data slicing circuit defining a threshold exceeding the signal envelope; and

a comparator arrangement configured to arranged and identify commencement of a header region by equating a first spike transition through the threshold as being indicative of the header region.

19. The DVD-RAM read channel of 18, wherein the comparator arrangement comprises first and second comparators respectively configured to process

opposite signal senses from the signal envelope, the first and second comparators each providing an output to a controller arranged to identify the relative signal level polarity between a first spike and a successive spike to identify a requirement for a phase reversal in a phase lock loop within the DVD-RAM read channel.